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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/723,169
Filing Date: November 26, 2003
Appellant(s): MULLIGAN ET AL.

Mr. Timothy Markison
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed April 21, 2006 appealing from the Office action mailed August 23, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,859,541	McMahan	1-1999
6,490,121	Pruett	12-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by McMahan et al. (US 5,859,541, hereinafter McMahan).

Regarding claim 1, McMahan discloses, in Figs. 3 and 4, a programmable driver comprises:

a first driver (42);

second driver (44) operably coupled parallel with the first driver to drive a signal (a signal from 48 to 49) on to a line (49) at a first drive level (a drive level when all drivers 42, 44, and 46 are ON) when a drive control signal (C1, C2, and C3) is in a first state (e.g. when n=3; C1=1, C2=0, C3=1; see col. 4, lines 30+) and wherein, when the drive control signal is in a second state (C1=0, C2=0, C3=0; see col. 4, lines 35+), the second driver is in a high-impedance state (since C1=0, the driver 44 is OFF which means it's in a high-impedance state) such that the first driver drives the signal (since C0=1, the driver 42 is ON and drives the signal) on the line at a second drive level (a drive level when only driver 42 is ON; see col. 4, lines 35+), wherein the first drive level is greater than the second drive level (the first drive level with all the drivers 42, 44, and 46 turned ON is greater than the second drive level with only one driver 42 is turned ON since more current flow through the drivers when more drivers are turned ON); and controller (52) operably coupled to generate the drive control signal based on load requirements of the line (col. 2, lines 36+).

Regarding claim 2, McMahan discloses, in Figs. 3 and 4, that wherein the first driver further comprises tri-state driver (42; col. 4, lines 39+) that is placed in a high impedance state (when 42 is disabled by C0=0) when an output enable signal (C0) is in a first state (logic 0) and

is placed in an active state (when 42 is enabled by C0=1) when the output enable signal is in a second state (logic 1).

Regarding claim 3, McMahan discloses, in Figs. 3 and 4, that wherein the controller (52) further functions to generate the drive control signal in the second state (C1=0, C2=0, C3=0) when the output enable signal (C0) is in the first state (logic 0).

Regarding claim 4, McMahan discloses, in Figs. 3 and 4, a third driver (46) operably coupled in parallel (see 46 and 42) with the first driver (42) to drive the signal on to the line at a third drive level (a drive level when C0=1, C1=0, C2=0, C3=1) when the drive control signal is a third state (C1=0, C2=0, C3=1) and wherein, when the drive control signal in the second state (C1=0, C2=0, C3=0), the third driver is in the high-impedance state (since C3=0, driver 46 is OFF), wherein the third drive level is greater than the second drive level (since one more driver, 46, is turned on for the third drive level which carries more drive current).

Regarding claim 5, McMahan discloses, in Figs. 3 and 4, that wherein the controller (52) further functions to: generate the drive control signal in the fourth state (C1=1, C2=1, C3=1), wherein, with the drive control signal in the fourth state, the first, second, and third drivers are coupled on parallel (see 42, 44, and 46) to drive the signal on the line at fourth drive level (a drive level when C0=1, C1=1, C2=1, C3=1), wherein the fourth drive level is greater than the third (since two more drivers are turned on for the fourth drive level which carries more drive current).

Regarding claim 6, McMahan discloses, in Figs. 3 and 4, that wherein the controller further functions to determine load requirement based on a load impedance on the line (col. 2, lines 36+; Claim 14) or an output signal strength setting.

Regarding claim 10, McMahan discloses, in Figs. 3 and 4, that wherein the controller comprises a state machine (col. 5, lines 10+) to generate the drive control signal based on the line drive requirement (col. 2, lines 36+; Claim 14).

Claims 7-9, 11, and 12 are essentially the same in scope as claims 1-6 and are rejected similarly.

Claims 13-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over McMahan in view of Pruett et al (US 6,490,121, "Pruett" hereinafter).

As applied previously, McMahan teaches all the features of the claimed invention, with the exception of teaching the claimed multiple function system on a chip integrated circuit comprises a plurality of interface modules, a converter, a processing module, and on-chip memory with their interconnections as claimed.

Pruett discloses a plurality of interface modules (176), a converter (190), a processing module (172), and on-chip memory (174) with their interconnections as claimed.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the driver of McMahan in the circuit 100 of Pruett in order to provide a programmable driver.

(10) Response to Argument

Appellant asserts, on page 5, that "McMahan does not disclose suggest or teach placing a second driver in a high-impedance state" and further asserts, on page 6, that "McMahan does not teach that the various buffers may be tri-stated (e.g., on, off, or in a high impedance state), but teaches that they the buffers are either connected via a coupling transistor to the output pin or not." However, McMahan teaches that the input at node 48 may be a data input (col. 4, lines

24+) which means data input can be either in logic 0 (OFF) or 1 (ON). Also, McMahan teaches that "control signals C0, C1, and Cn respectively function to couple each of buffers 42, 44, 46 to the output pin by controlling a coupling transistor within each of the buffers to couple the output of the buffer to the output pin (col. 4, lines 39+) and each of buffers 42, 44, and 46 may be implemented with any type of known buffer circuit structure (col. 4, lines 43+). Therefore, when any of the control signals C0, C1, and Cn are enabled, the buffer(s) associated with enabled control signal(s) C0, C1, and Cn will be connected by the coupling transistor(s) and the output of the buffer(s) will be either in logic 0 (1st state) or in logic 1 (2nd state) depending upon the state of the input signal at 48; and when any of the control signals C0, C1, and Cn are disabled, the buffer(s) associated with the disabled control signal(s) C0, C1, and Cn will be disconnected by the coupling transistor(s) and will be in high impedance state (3rd state). For example, when C1 is enabled, the second buffer 44 will be connected by the coupling transistor within the buffer 44. Therefore, the output of the buffer 44 will generate either 0 or 1 according to the data at 48. When C1 is disabled, the second buffer 44 will be disconnected by the coupling transistor within the buffer 44. Therefore, the output of the buffer 44 will be in high impedance state. Accordingly, the buffers may be tri-stated (logic 0, logic 1, and high impedance state).

Also, Appellant argues, on pages 5 and 6, that "McMahan does not disclose suggest or teach a configuration where the drive level is controlled in a first and second state between first and second drive levels". Appellant contends that controlling the output impedance of an output buffer as taught by McMahan is not the equivalent of, or suggestive of, controlling the drive level of the programmable driver of the present invention." However, according to the Ohm's Law, the output impedance of an output buffer is correlated with the drive level of the output

buffer. (For arguments sake, assume that the output impedance is equivalent to its resistance assuming that its net reactance is zero. See the following equation:

$Z = \sqrt{(R^2 + X^2)}$, where Z= impedance (Ω), R= resistance (Ω), X= net reactance (Ω)

$Z = \sqrt{(R^2 + X^2)} = \sqrt{(R^2 + 0)} = \sqrt{(R^2)} = R$)

Ohm's Law states that V = I x R, where V=Voltage, I=Current, and R=Resistance. Therefore, given that the power supply voltage is constant, when impedance or resistance decreases, the current increases; or visa versa. Accordingly, when less drivers (Z1-Zn) of McMahan turns on by control signals C_0-C_n, the higher impedance is present at the output pin 49 (col. 4, lines 30+), and when more drivers (Z1-Zn) of McMahan turns on by control signals C_0-C_n, the lower impedance is present at the output pin 49. When lower impedance is present at the output pin, the more current is driven at the output pin according to the Ohm's Law. Therefore, McMahan implicitly teaches a configuration where the drive level is controlled in a first and second state between first and second drive levels.

Appellant further contends, on pages 6 and 7, that "McMahan does not address, teach, or suggest generating a control signal based on the load requirements of the programmable driver as is presently claimed in claim 1, but teaches generating control signals based of a desired output impedance." However, McMahan teaches in col. 2, lines 36+ that "Since the load of an output buffer of a data processor approximates a transmission line at high frequencies, a reflection may occur at the end of the line which may result in ringing and a significant reduction in noise margin. Therefore, a proper impedance value of an output driver circuit of a data processor will prevent undesired reflections of a voltage waveform provided at the output of the data processor." McMahan further teaches in Claim 14 that user of the circuit is allowed "to select a

value of the control signal to permit the user of the circuit to select one of a plurality of predetermined, discrete output impedance values for the output terminal of the circuit". Therefore, it can be concluded that the user can select a value of the control signal based on the load requirements, so that the controller operably coupled to generate the drive control signal (C1-Cn) based on load requirements of the line", as set forth in claim 1.

Appellant's argument regarding claims 13 and 19 are equally applicable to claims 1 and 7 discussed above and will not be repeated.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Daniel Chang

DANIEL CHANG
PRIMARY EXAMINER

Conferees:

R.B

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